CMOS Backplane Technology
For
Micro-LED AR Display

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Sapien Semiconductors Inc
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Augmented Reality (AR) is Primed To Scale

- Facebook, Apple, & Samsung have increased their investment in AR hardware devices.
- By 2022, it is expected that consumer-grade AR headsets should turbocharge this trend.
- From 2025, Micro-LED display will see meaningful volume of the mass production

Source: Yole Developpement Report, 2021
**AR Micro-Display**

- Display size: 0.3” or smaller with RGB
- Higher than 2,000 PPI
- Monolithic hybridization

<table>
<thead>
<tr>
<th></th>
<th>PPI</th>
<th>Sub-pixel Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>4K 55” TV</td>
<td>80</td>
<td>&gt; 100 μm</td>
</tr>
<tr>
<td>Smart Watch</td>
<td>300</td>
<td>24 ~ 34 μm</td>
</tr>
<tr>
<td>Smartphone</td>
<td>500</td>
<td>14 ~ 21 μm</td>
</tr>
<tr>
<td>VR</td>
<td>500-1,500</td>
<td>6 ~ 17 μm</td>
</tr>
<tr>
<td>AR/MR</td>
<td>&gt; 2,000</td>
<td>&lt; 3 μm</td>
</tr>
</tbody>
</table>
## SWOT on Micro-LED Display

- Early adoption on 2021, and significant adoption rate by 2025
- RGB solution should be addressed

<table>
<thead>
<tr>
<th>Strength</th>
<th>Weakness</th>
</tr>
</thead>
<tbody>
<tr>
<td>• High brightness</td>
<td>• Monolithic arrays</td>
</tr>
<tr>
<td>• High pixel density</td>
<td>– no repairability</td>
</tr>
<tr>
<td>• Low power consumption</td>
<td>– Yield issue</td>
</tr>
<tr>
<td>• Small dimensions for micro-displays</td>
<td>• Full color (RGB) &amp; beam shaping are very challenging</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Opportunity</th>
<th>Threats</th>
</tr>
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<tbody>
<tr>
<td>• High brightness is a strong differentiator which is a must for high-end devices.</td>
<td>• Further improvement of OLED micro-displays in brightness</td>
</tr>
<tr>
<td>• Major investment by big players such as Facebook, Apple, Microsoft, and et el.</td>
<td></td>
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Micro-LEDs

- LEDs are categorized by its size which then dictates packaging solution & its applications
- Micro-LEDs are a “disruptive” evolution, not an “incremental” evolution

### LED Chip Size

- **Traditional LEDs**: >1 mm, 1 mm, 200 µm
- **“Mini-LEDs”**: 100 µm, 50 µm, 30 µm, 10 µm, 2 µm
- **“Micro-LEDs”**: 150 µm, Limit: ~50-100 µm

### Packages

- **Assembly**: SMD, through hole (smallest size: 0.5 x 0.5 mm²)
- **“Mini-LEDs”**: SMD/Chip on Board
- **“Micro-LEDs”**: Package-free: “Chip On Board” only

Source: Yole Development Report
# CMOS Backplane, LED, & Integration

## Current Technology (Problem)

**CMOS Backplane**
- Wafer: 8"
- HV CMOS Process
- PAM driving

**LED**
- Mini-LED & 2D
- Wafer size: 2", 4", or 6"
- GaN-on-Sapphire

**Integration**
- Singulate LEDs (R/G/B) from each LED wafers, and mass transfer (such as Pick & Place) to a target substrate

## Disruptive Technology (Solution)

**CMOS Backplane**
- Wafer: 12"
- CMOS Logic process
- PWM driving w/ Memory-inside-Pixel

**LED**
- Micro-/Nano-LED & 3D
- Wafer Size: 8" or 12"
- GaN-on-Silicon

**Integration**
- Wafer-to-Wafer hybridization or Cu-to-Cu bonding
- 3D Heterogeneous integration
CMOS Backplane, LED, & Integration

- Wafer-to-Wafer hybridization needs a special process requirement on CMOS Backplane

<table>
<thead>
<tr>
<th>Technology or Solution</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMOS Backplane</strong></td>
<td></td>
</tr>
<tr>
<td>- Post-processing readiness for wafer-to-wafer hybridization</td>
<td>- Pixel size: as small as 2 or 3 μm pitch</td>
</tr>
<tr>
<td>- CMOS foundries: 40nm/28nm CMOS process with 3.3V/5V transistors</td>
<td>- Leverage CMOS foundry for mass production facility</td>
</tr>
<tr>
<td></td>
<td>- Cost reduction</td>
</tr>
<tr>
<td><strong>Micro-LED</strong></td>
<td></td>
</tr>
<tr>
<td>- GaN-on-Silicon</td>
<td>- Nano/Micro-LEDs</td>
</tr>
<tr>
<td>- Aledia, Plessey, Samsung, Allos, &amp; Toshiba</td>
<td>- Higher yield</td>
</tr>
<tr>
<td></td>
<td>- 8” or 12” wafer</td>
</tr>
<tr>
<td></td>
<td>- 30~50% cost reduction (GaN-on-Si vs. GaN-on-Sapphire)</td>
</tr>
<tr>
<td><strong>Integration</strong></td>
<td></td>
</tr>
<tr>
<td>- Wafer-to-Wafer Hybridization by CMOS foundries</td>
<td>- Leverage a stacking processes</td>
</tr>
<tr>
<td>- Aledia, Plessey, Samsung &amp; et al.</td>
<td>- Mass production</td>
</tr>
<tr>
<td></td>
<td>- 3-Dimensional structure</td>
</tr>
<tr>
<td></td>
<td>- Various target substrates</td>
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</table>
Micro-LED Transfer Technology

Mass Transfer Technology

Monolithic integration techniques

Source: Micro-LED with quantum dots in display technology, by Zhaojun Liu
Challenges on AR CMOS Backplane

- **Target resolution**: HD+ or higher with RGB
- **Pixel size**: < 3µm pitch per sub-pixel
- **Embedded memory**: frame buffer memory, OTP, or flash memory
- **Thermal management of finished module**: affected by the # of LEDs and its efficiency
- **Integration** with LED array/wafer: Heterogeneous hybridization
- **Testability**: wafer test or module test?
- **Display image compensation**: De-mura, Dead-pixel compensation, & other yield improvement
AR CMOS Backplane

- **Pixel driver:**
  - PWM driving with constant current source
  - MIP (Memory-inside-pixel)
- **Integration w/ LED wafer:** Top metal layer structure of CMOS wafer
- **28nm or finer process is desirable in order to meet pixel size and power consumption**

**Block Diagram of Pixel Driver**

**Minimum Achievable Pitch (µm) for Sub-pixel**

<table>
<thead>
<tr>
<th>Process Node</th>
<th>10-bit MIP-based Digital (PWM) Driving</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.18 µm @ 8&quot;</td>
<td>12</td>
</tr>
<tr>
<td>40 nm</td>
<td>3</td>
</tr>
<tr>
<td>28 nm</td>
<td>2</td>
</tr>
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Key Functions of AR CMOS Backplane

**Key Functions**

- **Pixel circuit**
  - SRAM memory inside
  - PWM Driving Scheme w/ Brightness Control
- Layout technique to squeeze the pixel size
- Ultra low power architecture
- Image processing IPs: Compression, Gamut, De-mura, scaler
- Dead-pixel compensation IPs
- High-speed serial interface IPs: MiPi
- Testability
Thank You!